CLAIMS:

1. A method for high speed addressing of memory locations within the same page by accessing a first selected location in the memory space using at least a first and a second part of the address of the selected location, the method comprising the steps of:

(a) transmitting a first part of the address of a second selected location in the memory space;

(b) determining whether at least a second part of the address of said second selected location corresponding to the second part of the address of the first selected location is the same as the second part of the address of the first selected location; and

(c) determining the address for said second selected location without transmitting said second part of the address of said second selected location by joining the second part of the address of the first selected location with said first part of the address of said second location on the condition that said second part of the address of said second selected location is the same as the said second part of the address of the first selected location as determined in step (b).

2. The method of claim 1, further comprising storing the second part of the address of the first selected location in a register in the memory.

3. The method of claim 2, further comprising providing an Address Enable signal that is active during at least part of step (a), wherein step (b) includes determining whether said Address Enable signal is inactive.

4. The method of claim 1, wherein said first and second parts of the address of the first and said second selected location are of equal size.

5. The method of claim 2, wherein said first and second parts of the address of the first and said second selected location are of equal size.

6. The method of claim 3, said first and second parts of the address of the first and said second selected location are of equal size.

7. An apparatus for high speed addressing of a memory locations within the same page by accessing a first selected location in the memory space using at least a first and a second part of the address of the selected location, the apparatus comprising a logic circuit adapted to perform a method comprising the steps of:

(a) transmitting a first part of the address of a second selected location in the memory space;

(b) determining whether at least a second part of the address of said second selected location corresponding to the second part of the address of the first selected location is the same as the second part of the address of the first selected location; and

(c) determining the address for said second selected location without transmitting said second part of the address of said second selected location by joining the second part of the address of the first selected location with said first part of the address of said second location on the condition that said second part of the address of said second selected location is the same as the said second part of the address of the first selected location as determined in step (b).

8. The apparatus of claim 7 adapted to store the second part of the address of the first selected location in a register in the memory.

9. The apparatus of claim 8, wherein said logic circuit is further adapted to receive an Address Enable signal that is active during at least part of step (a), wherein said logic circuit is further adapted so that step (b) includes determining whether said Address Enable signal is inactive.

10. The apparatus of claim 7 adapted so that said first and second parts of the address of the first and said second selected location are of equal size.

11. The apparatus of claim 8 adapted so that said first and second parts of the address of the first and said second selected location are of equal size.

12. The apparatus of claim 9 adapted so that said first and second parts of the address of the first and said second selected location are of equal size.

13. A machine readable medium embodying a program of instructions for execution by a machine to perform a method for high speed addressing of memory locations within the same page by accessing a first selected location in the memory space using at least a first and a second part of the address of the selected location, the method comprising the steps of:

(a) transmitting a first part of the address of a second selected location in the memory space;

(b) determining whether at least a second part of the address of said second selected location corresponding to the second part of the address of the first selected location is the same as the second part of the address of the first selected location; and

(c) determining the address for said second selected location without transmitting said second part of the address of said second selected location by joining

the second part of the address of the first selected location with said first part of the address of said second location on the condition that said second part of the address of said second selected location is the same as the said second part of the address of the first selected location as determined in step (b).

14. The machine readable medium of claim 13 adapted so that the method further comprising storing the second part of the address of the first selected location in a register in the memory.

15. The machine readable medium of claim 14 adapted so that the method further comprises providing an Address Enable signal that is active during at least part of step (a), wherein step (b) includes determining whether said Address Enable signal is inactive.

16. The machine readable medium of claim 13 adapted so that said first and second parts of the address of the first and said second selected location are of equal size.

17. The machine readable medium of claim 14 adapted so that said first and second parts of the address of the first and said second selected location are of equal size.

18. The machine readable medium of claim 15 adapted so that said first and second parts of the address of the first and said second selected location are of equal size.

19. The machine readable medium of claim 16 adapted so that said first and second parts of the address of the first and second selected locations are each 8 bits.

20. The machine readable medium of claim 18 adapted so that said first and second parts of the address of the first and second selected locations are each 8 bits.